International Journal Of Advanced Research In Engineering Technology & Sciences
ISSN: 2394-2819
Email: editor@ijarets.org March- 2015 Volume 2, Issue-3 www.ijarets.org

An Innovative Design and Implementation of the DDR2/DDR3/DDR4 SDRAM Compatible Controller

Ayush Garg
B.Tech Student
Department of ECE
SRM University NCR Campus
Modinagar

Pankaj Agarwal
Assistant Professor
Department of ECE
SRM University NCR Campus
Modinagar

ABSTRACT—
With the rapid increases of computer performance in recent years, the frequency and performance of memory are required to be higher and higher. Just using DDR2 SDRAM, we can't meet the demands. Compared with DDR2, DDR3, DDR4 SDRAM.(DDR4) has higher speed, lower power, higher efficiency. A recent statistics shows that DDR4 will replace DDR3 and DDR3 will replace DDR2 and DDR2 will replace DDR in last several years with a 3-4 years gap, but DDR /DDR2/DDR3 is still prevailing today. For this reason, based on a common standard bus interface, an innovative design of the DDR2/DDR3/DDR4 SDRAM compatible controller is implemented. If this compatible controller can be included in the several architectures, the system will be more flexible and transplantable. Besides, during the period when DDR2 is replaced by DDR3/DDR4, using this controller will greatly shorten time to market, lessen manual work and reduce product cost. Based on a common standard bus interface, an innovative design of the DDR2/DDR3/DDR4 SDRAM compatible controller is implemented. This controller maximize a channel bandwidth, more flexible, and minimizes access latencies through efficient request scheduling, refresh schemes.

Keywords—DDR2/3/4SDRAM, Compatible controller, Verilog **xilink 14.7**

I. INTRODUCTION

It is well known that memory is an essential part in the whole computer systems and several digital architectures. Compared with the rapid development of CPU, the development of memory is much slower .it is reported that the gap between core and arm SDRAM is growing at 60%/year. The bottle -neck existed between CPU and memory slows down the improvement in computer performance. The performance and architectural efficiency of memory are required to be increased DDR2/3/4 in 2004,2007,2012.these having higher speeds, low power, high efficiency and self refresh functioning, according to a recent surveys, in late some years the percentage of DDR2 will decreases to 50% but DDR3/DDR4 will rise to 45-55. A recent static shows that DDR3/DDR4 will replaceDDR2/DD Rin recent two or last years, but DDR2/DDR3/DDR4 is still prevailing today. This article provides a comprehensive and detailed analysis DDR2, DDR3 and DDR4 and then, a new design of the DDR2/DDR3/DDR4 compatible controller based on a common standard bus interface is implemented and verified. If this controller can be applied in the computer, it will be very useful during the period when DDR2 is replaced by DDR3 and DDR4.

II. ANALYSIS AND COMPARISONS BETWEEN DDR2,DDR3 AND DDR4

1) DDR2 SDRAM CONTROLLER

DDR2 is the next generation of memory developed after DDR. DDR2 increased the data transfer rate referred to as bandwidth by increasing the operational frequency to match the high FSB frequencies and by doubling the prefetch data rate. There will be more about the memory prefetch buffer data rate later in this section. DDR2 operates at 1.8 volts. The lower voltage counters the heat effect of the higher frequency data transfer. DRR operates at 2.5 volts. DDR2 uses a different motherboard socket than DDR, and is not compatible with

motherboards designed for DDR. If the DDR2 is forced into the DDR socket, it will damage the socket and the memory will be exposed to a high voltage level.

2) DDR3 SDRAM CONTROLLER

DDR3 was the next generation memory introduced in the summer of 2007 as the natural successor to DDR2.DDR3 increased the pre-fetch buffer size to 8-bits an increased the operating frequency once again resulting in high data transfer rates than its predecessor DDR2. In addition, to the increased data transfer rate memory chip voltage level was lowered to 1.5 V to counter the heating effects of the high frequency. By now you can see the trend of memory to increase pre-fetch buffer size and chip operating frequency, and lowering the operational voltage level to counter heat. DDR3 is both electrical and physically incompatible with previous versions of RAM. In addition to high frequency and lower applied voltage level, the DDR3 has a memory reset option which DDR2 and DDR1 do not. The memory reset allows the memory to be cleared by a software reset action. Other memory types do not have this feature which means the memory state is uncertain after a system reboot. The memory reset feature insures that the memory will be clean or empty after a system reboot. This feature will result in a more stable memory system.

3) DDR4 SDRAM CONTROLLER

DDR4 was the next generation memory introduced in 2012 as the natural successor to DDR3.DDR4 increased the pre-fetch buffer size to 16-bits an increased the operating frequency once again resulting in high data transfer rates than its predecessor DDR3. In addition, to the increased data transfer rate memory chip voltage level was lowered to 1.2V

In addition to high frequency and lower applied voltage level, the DDR4 has a memory reset option which DDR2 and DDR1 do not. DDR4 delivers higher performance at a higher speed than DDR2 and DDR3. DDR4 can achieve more than 2 Gbps per pin beyond 30 Gbps bandwidth.

III. . THE DESIGN OF MEMORY CONTROLLER

The functions that DDR2/3/4 memory controller needs to be done include: to receive and process the memory access requests, memory self-test operation, memory refresh and initialization operation, implementation of CPU register access path, read and write of all register in DDR2/3/4 controller. The process of DDR2/3/4 controller for memory access requests is: receiving all kinds of requests and scheduling the memory access according to the priority of their quest, generating the correct memory address control signal sin accordance with the selected request and finishing the sending and accepting of memory data.

1) Overall Structure

The DDR2/3/4 memory controller that we designed is comprised of register control module, memory access control module, memory access data path module and DDR3SDRAM interface module, the structure is showed in as Figure 1.

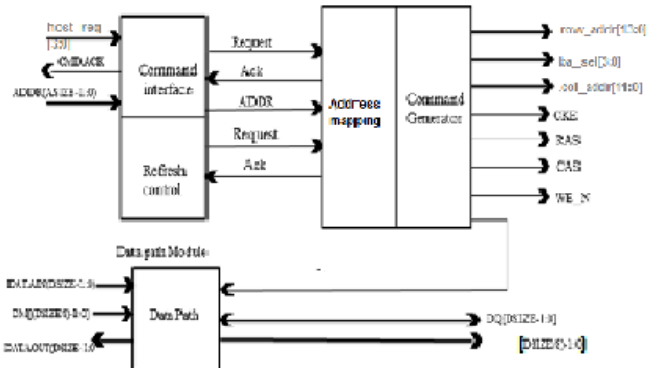

Fig.1 controller structure

Command control module consists of memory initialization sequence logic, self-test control logic, read and write control logic of all registers in DDR3 controller.Address mapping module implements memory scheduling logic. Memory access data path module is used to control the input and output of the memory data. DDR2/3/4 interface module implements the physical interface of memory, includes transmission of address and command, data transmission and generation of memory clock signal. Because command control module is the key part of DDR2/3/4 compatible controller, we will focus on it.

2) Structure and function of control interface and refresh module

Control_interface_and_refresh managment module Control Interface Module accepts command from embedded system and decoding the command and providing the request to the command module. For decoding a command an arbiter is used.

Refresh management

DDR2/3/4 SDRAM memories require a refresh of all rows in any rolling 64 ms. the refresh in normal operating mode is done by issuing an auto refresh command. Up to eight auto refresh commands can be issued one after another and the time interval to the next refresh command will be extended accordingly. Within the controller, the circuit to flag the Auto Refresh Command is built. With the help of system clock, to make the counter refresh a 11,333 times counter run to make a refresh signal.

Algorithm Steps

1) Divide the memory (host) requests in collection into8groups 0 -7 according to bank address, making the bank address of memory requests in-group;
2) Choose the request with earliest arrival time in-groups the current candidate request;
3) Sequentially solving the minimum interval between the current candidate request and six times prior;
4) Find the scheduled time of current candidate request;
5) Prior consideration of the memory bank has not been accessed after F cycles, determine the request should be scheduled;
6) remove the selected request from corresponding request group;
7) update the beat counter for scheduling of each memory bank;
8) Repeat above steps 2-7, until all memory access scheduling is completed;
9) Return Memory access scheduling policy is implemented in memory access scheduling module, which determines the performance of the memory controller.

3) Data Path

One of the most difficult aspects of DDR controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path.

4) Command controller module

The controller consists of a state machine which performs DDR read and write accesses based on user interface request. The controller consists of a high performance timing & control state machine that observes all timing requirements and issues the commands to the memory devices at the shorted time possible. The DDR controller consists of a high performance memory controller for system requiring access to external devices with lowest latency and highest throughput. The controller accepts and decodes user interface commands and generates read, write, refresh commands.

1) After completion of initialization, there is only refresh request, self-test request initiated by CPU and memory access requests can be scheduled, according to the priority order of refresh request, self-test request and memory access request.
2) If exists a refresh request, the request can be scheduled after completion of current operation, and the process other self-test and memory access request;

3) If exists a self-test request, the request can be scheduled after completion of current operation, and the process other memory access request;

5) Address mapping module

The address mapping module gets its control signals from the controller, and generates row, column, and bank addresses for the DDRx SDRAM. The address mapping also generates burst, burst length cas, ras values for the burst counter (brst_cntr) . The controller generates address and control lines on the negative edge of clk. What makes it possible to interface between user and DDRX SDRAM w when performing mode register command module address is used to set operating condition for DDRX SDRAM?

Memory control module is the most critical part in the memory controller. As the memory chip has 8 banks, in order to solve the problem of address conflicts as well as to facilitate to implement multi-bank concurrent scheduling, memory access requests are divided into eight request groups in accordance with their bank address before scheduling, then schedule is carried out among the eight requests.

Initialization sequence request only run once at system startup and can generate pre-charge, load mode register and refresh requests. Upon completion of initialization, automatically refresh request, self-test request initiated by CPU and memory access requests must be sent to the memory access scheduling module, and then memory access control signal generation module generate memory access control signals for selected request, including the address control signal, data strobe control signal, and read and write control signal. Memory access control signals are then sent to the DDR2/3/4 SDRAM interface to generate DIMM memory physical interface signals.

IV. SIMULATION AND SYNTHESIS

Connecting the compatible controller, bus interface and the simulation models together, we can simulate over design. The controller is written in verilog language, the simulator uses isim simulator, simulation results of all the five blocks are shown individually. The results consist of the simulation of the controller. The syntax of the RTL design is checked by using Xilinx

Fig. 2 DDR2/3/4 SDRAM compatible WRITE

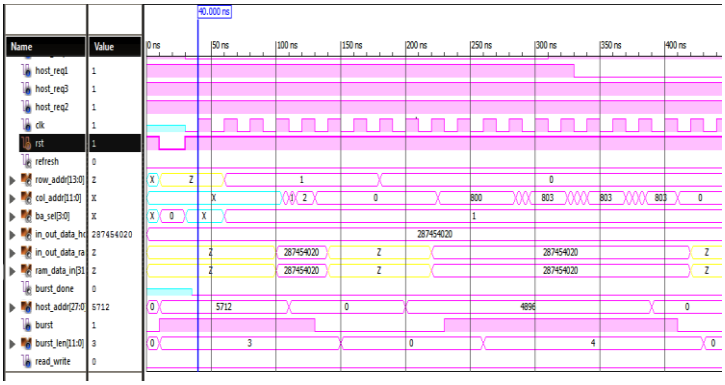

Fig 3 DDR2/3/4 SDRAM compatible READ

After simulation the controller is synthesized. Using Xilinx tool, the synthesized result shows that with this compatible controller, we can obtain the access of 2.90GHZ operating frequency of compatible controller and the transfer rate is 490 mbps for DDR2 SDRAM and 930 mbps for DDR3 SDRAM and 1800mbps for DDR4 SDRAM.

V. CONCLUSION

As we have said above, the I/O interface of DDR2, DDR3 and DDR4 is different. Compatible motherboards have been published by now. To takeECS915P as an example, it can support both DDR2 SDRAM memory and DDR3 SDRAM memory. To sum up, with the current promotion of computer, in order to meet the demand of the market, there is a growing trend towards the design with the feature of good performance, high flexibility, high extensibility, easy reuse and low cost. Memory will continue to playan inevitably crucial role in the computer field. For this reason, an innovative design and implementation of theDDR2/DDR3/DDR4compatible controller is presented in this paper. Using the compatible controller we designed here, motherboards whether support DDR2 or DDR3 or DDR4 can be accessed correctively and effectively. Therefore, if this compatible controller can be introduced in the computer architecture, the system will be more flexible and transplantable. Besides that, since DDR4 will inevitably take the place of DDR3 and DDR3 take the place of DDR2 in recent years, then using this compatible controller will greatly shorten time to market, lessen manual work and reduce cost.

VI. REFERENCES

1. Priyanka Bibay, Anil kumar sahu, " Design and implementation ofDDR SDRAM Controller using verilog " IJSR 2013.
2. Jian Qituo, Liu Liansheng,Peng Yu , "Optimized FPGA based DDR2 SDRAM Controller" IEEE 2013.
3. Darshan Makam, Jayashree H.V, "An Innovative Design of the DDRl/DDR2 SDRAM Compatible Controller" IEEE 2011.
4. Synthesizable DDR SDRAM controller, Application note, 2002. (Xilinx- Inc., XAPP200)
5. K. Lahiri, A. Raghunathan, Ganesh lakshminarayana ,"The LOTTERYBUS on-chip Communication architecture", IEEE Trans. On VLSI system, June 2006.
6. Guo Li, Zhang Ying, Li Ning, and Guo Yang, "TheFeature of DDR SDRAM and the Implementation of DDR SDRAM Controllers via VHDL",The Journal of China Universities of Posts and Telecommunications, 2002, vol.9,no. 1, pp. 61-65.
7. J. Breckling, Ed., The Analysis of Directional Time Series: Applicationsto Wind Speed and Direction, ser. Lecture Notes in Statistics. Berlin, Germany: Springer, 1989, vol. 61.
8. S. Zhang, C. Zhu, J. K. O. Sin, and P. K. T. Mok, "A novel ultrathin elevated channel low-temperature poly-Si TFT," IEEE Electron DeviceLett., vol. 20, pp. 569–571, Nov. 1999.
9. M. Wegmuller, J. P. von der Weid, P. Oberson, and N. Gisin, "High resolution fiber distributed measurements with coherent OFDR," in Proc. ECOC'00, 2000, paper 11.3.4, p. 109.
10. R. E. Sorace, V. S. Reinhardt, and S. A. Vaughn, "High-speed digital-to-RF converter," U.S. Patent 5 668 842, Sept. 16, 1997.